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(54) Digital hearing aid system

(57) A hearing aid (12,14), having alterable parameters, includes analog-to-digital input circuitry (30) for forming a digital signal representative of an incident acoustic wave. A digital signal processor (32), coupled to said input circuitry (30), forms and processes, at a first rate, first and second frequency distinguishable data streams representative, at least in part, of the digital signal. A control unit (34) coupled to said processor (32) includes circuitry for logarithmically processing at least one of the digital data streams, at a reduced rate which is less than the first rate. A parameter value storage memory (34b) is coupled to the unit (34), and an interface (38) is provided for accessing the memory (34b) and altering parametric values stored therein.

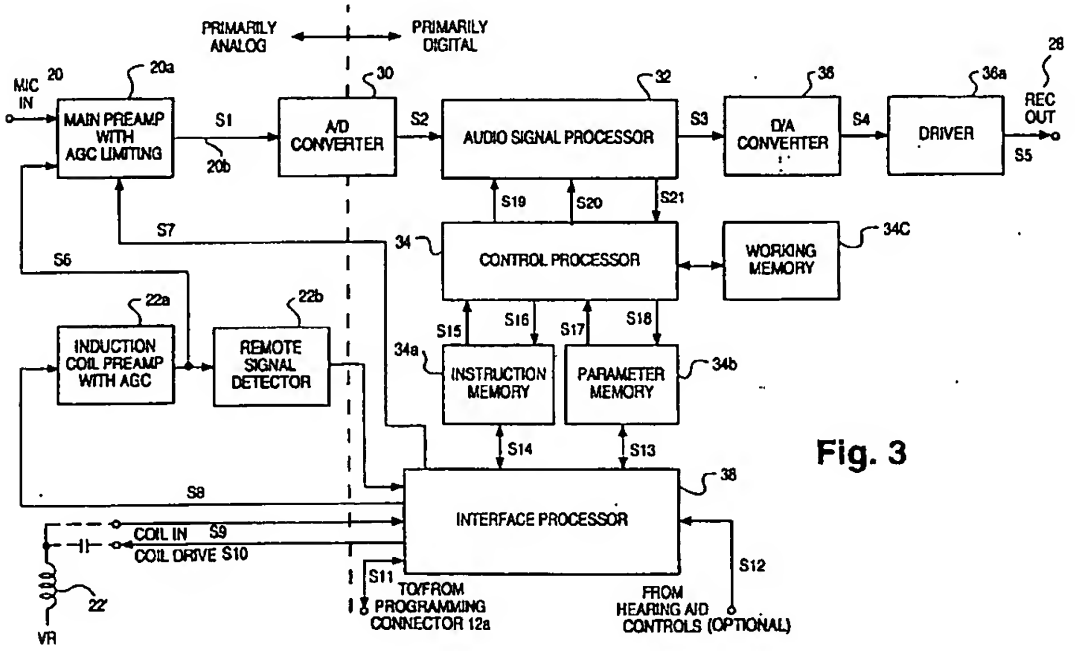

Fig. 3

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Description

The invention pertains to electronic hearing aids. More particularly, the invention pertains to hearing aids which incorporate digital signal processors for processing and amplifying incident acoustic waves as well as equipment for programming such hearing aids.

Known forms of electronic hearing aids incorporate circuitry for the purpose of processing and amplifying an incident acoustic wave. The nature of the processing and the degree of amplification that is appropriate varies widely from one individual to another.

There has been and continues to be an ongoing need for electronic systems and hearing aids which in addition to providing appropriate levels of gain and/or other processing provide for ready modification of processing characteristics so that standardized circuitry can be used to meet the needs of a wide variety of users. Additionally, the auditory characteristics of any given individual vary over a period of time and it would be particularly useful to be able to alter processing characteristics or parameters thereof after delivery and use of the hearing aid as experience is gained with it. It would also be desirable to rapidly and directly compare the effects of such modifications.

It would be especially beneficial if such processing characteristics and related parameters could be modified in real-time while the hearing aid is actually in use so as to maximize the beneficial effects for the actual user. Further, it would be desirable to be able to incorporate the benefits of digital signal processing which can be carried out at relatively high rates on the one hand with control methods or algorithms which might allow processing at a lower rate so as to achieve a more optimum result for the user.

Further, it would be desirable to be able to carry out the complex calculations necessary for signal processing without having to make extensive use of multiplication and division operations which tend to take longer than simpler operations such as addition or subtraction. Finally, there continues to be a need to carry out signal processing which will increase the intelligibility of speech relative to noise which is always present in the environment.

In accordance with an embodiment of a first aspect of the present invention, an input transducer which converts an incident audio wave to an electrical signal is combined with an analog-to-digital converter, a digital signal processor, a control unit coupled to the digital signal processor and an output transducer which carries out a low-pass filter function simultaneously with generating an audible output wave. The digital signal processor incorporates a low-pass digital filter in combination with a high-pass digital filter. The filters, in one aspect of the invention, include one or more programmable corner frequencies.

Digitized outputs from the filters are combined in a summing stage. An output signal from the summing stage is converted to an analog form in a digital-to-analog converter and used to drive an output transducer which also carries out a low-frequency filtering operation.

In another aspect of the invention, a sigma-delta analog-to-digital converter is coupled between the input transducer and the digital signal processor. A decimation circuit can be coupled between the output of the converter and inputs to the signal paths of the dual digital filters.

In yet another aspect of the invention, gain control can be accomplished in the signal path by multiplying a digital multi-bit gain control signal by a one or two bit representation of the digitized input signal, where there is no decimation circuitry. Alternately, multiplication can be by a three to four bit representation of the digital input signal in the case of a circuit which carries out a decimation function by a factor of 2.

In yet another aspect of the invention, the digital filters can be operated at high oversampling rates and can provide adjustable characteristic frequencies determined by filter coefficients which are binary based. The use of binary based filter coefficients eliminates any need for multipliers. Multiplication can be carried out by using shift operations. These could be implemented using multiplexer circuits for variable multiplications and hard wired offsets for fixed multiplications.

In yet another aspect of the invention, the output digital-to-analog converter can be implemented without needing any additional filters beyond the low - pass characteristic of the output transducer.

In yet another aspect of the invention, signal amplitudes which have been digitized can be converted to logarithmic form. In logarithmic form, additions and subtractions replace multiplications and divisions. Multiplication steps can be used to approximate exponential functions.

In yet another aspect of the invention, circuit simplicity is promoted by use of a piecewise linear approximation to a logarithmic function. After processing, the resulting signals are converted back to a linear domain using a piecewise linear approximation to an exponential function.

By translating various of the control signals to a logarithmic representation, not only is circuit complexity reduced, but the logarithmic domain readily supports a wide dynamic range very efficiently. As a result, dual input compression systems, dual output compression systems and a noise reduction system can be provided for each of the frequency bands and can be independently adjustable.

In yet another aspect of the invention, the hearing aid can include a programmable processor wherein control instructions can be stored in nonvolatile instruction memory when the unit is manufactured. This allows units to be built with different sets of instructions implementing different signal processing algorithms.

In yet another aspect of the invention, one or more

interfaces can be provided to enable the control unit to communicate with external circuitry. In one aspect, the interface can be directly coupled to an external programming apparatus for the purpose of reading out the values of parameters stored within the hearing aid and for adjusting parameters.

In yet another aspect of the invention, a remote control unit can be provided. Such a unit could transmit a modulated RF carrier which could be detected by the interface of the hearing aid. Such an arrangement would make it possible to remotely control parameters of the aid so as to optimize performance thereof in view of the individual characteristics of a user and of the specific listening situation.

The remote control unit can be coupled with a computer for the purpose of adjusting each of a number of sets of parameters stored within the remote control unit.

Further, in accordance with the yet another aspect of the invention, a plurality of parameters are field programmable for each of the channels of the digital signal processor. Such parameters can be established or modified based on user characteristics as a result of being field programmable. As user characteristics vary over time, the parameters may be readily altered to take such variations into account.

A digital hearing aid in accordance with another aspect of the invention incorporates a sigma-delta A/D converter with either no decimation or with decimation by a factor of 2. This reduces substantially the amount of digital signal processing needed for decimation filtering.

Further, using a sigma-delta A/D converter in which pulse width modulation (return-to-zero coding) is used in the digital feedback path eliminates the problem of inaccuracy and noise caused by unequal rise and fall times.

Gain control can be accomplished by multiplying a digital multibit gain control signal by a 1 or 2 bit representation of the digital input signal (in the case of no decimation) or by a 3 or 4 bit representation of the digital input signal (in the case of decimation by a factor of 2). This reduces substantially the complexity of the multiplier.

Using infinite impulse response (IIR) digital filters designed to operate at high oversampling rates and providing adjustable characteristic frequencies determined by filter coefficients that have values of 2^{-n}, where n is an integer eliminates the need for multipliers, since the coefficients can be implemented as digital shifts.

Using a sigma-delta D/A converter to produce an output bit stream with no signal reconstruction filter, relying on the low pass characteristic of the output transducer to filter out high frequency components and relying on the inductive impedance of the output transducer to achieve high efficiency eliminates the need for a reconstruction filter and provides a highly efficient output drive to a magnetic transducer.

A digital hearing aid embodying yet another aspect of the invention uses a digitally rectified, filtered, and decimated version of the output signal in each frequency band to represent the signal amplitude in that band. Digital implementation of these functions is accurate and efficient and requires no off-chip components. Decimation to a low sampling rate allows the control path to operate at a much reduced computation rate.

Converting signal amplitude to a logarithmic domain using a piecewise linear approximation to a logarithmic function and then, after processing these signals using a control algorithm, converting the resulting control signals back to the linear domain using a piecewise linear approximation to an exponential function reduces hardware requirements. Multiplications and divisions are replaced by additions and subtractions and exponentials are replaced by rudimentary multiplications, greatly reducing circuit complexity. Also, the logarithmic domain expresses a wide dynamic range very efficiently. This allows providing enough capability to provide a dual input compression system, a dual output compression system, and a noise reduction system, with each of these independently adjustable for each of two frequency bands.

A control processor that concurrently performs the operations of selection of two input operands, multiplication or shift, addition or subtraction or conditional selection, and output storage allows more processing per cycle than consecutive operation.

Implementing a control algorithm using instructions programmed into a non-volatile instruction memory at the time of manufacture of the hearing aid permits rapid implementation of corrections or improvements in the control algorithm.

A hearing aid with a digital serial interface in accordance with the present invention can use pulse width modulation (return-to-zero coding) for the transmitted data. As a result, the transmitted signal is self clocking so that a separate clock line is not needed and timing is not critical. Also, since only a single signal line is used, it is readily adaptable to wireless communication.

A hearing aid that uses a serial interface can provide some or all of the following functions:

a) Programming hearing aid signal processing parameters
b) Reading out parameters from the hearing aid
c) Remote control of the signal processing parameters and other control settings, such as volume control
d) Programming the instruction memory
e) Reading out the instruction memory

Using a single interface for these functions reduces cost and complexity.

A hearing aid with a serial interface that includes an antenna switch and a carrier modulator so that the same tuned coil can be used as both a receive and transmit antenna. This permits wireless transmission in both di-

rections, eliminating the need for a programming connector. A single tuned coil antenna, saves cost and space. 50kHz pulse width modulation transfers a binary bit stream.

A remote control for a hearing aid that embodies the present invention can use pulse width modulation of a 50kHz induction field (RF) carrier for data transmission. The carrier frequency is well beyond the audio band to minimize audible interference, but still below allocated frequencies. The induction field is not subject to body shadow effects and allows control of both hearing aids in a binaural fitting from the same remote control location. Pulse modulation allows highly efficient output stage.

A remote control for a hearing aid that embodies the present invention can use two transmitting coils in space quadrature, driven with carriers in phase quadrature. This minimizes nulls in the pickup pattern of the transmitted signal.

In a further aspect of the invention, a remote control for a hearing aid can use a conditioning pulse and a transmitted identification number to signal a valid transmission for the hearing aid being controlled. This minimizes false actuation or actuation by another user and permits independent control of both hearing aids of a binaural pair.

A remote control that uses tuned coils driven by a bridge type output in a switching mode provides high transmitter efficiency.

In a further aspect of the invention, a remote control having a programming connector enables a computer to program multiple memories in the remote control and that also enables a computer to program memories in the hearing aid using wireless transmission from the remote control to the hearing aid. Hence, wireless programming of the hearing aid can be effected using the modulator and transmitter already existing in the remote control.

In a further aspect of the invention, a hearing aid with a remote control that uses the same induction coil for receiving the remote control signal and for telephone induction pickup and induction loop pick up has reduced space requirements and cost. This remote control uses the same low frequency RF transmission for both the phone and remote control scheme. Both uses the same coil in and out.

A hearing aid for use with this remote control uses AGC acting on the tuned receiver coil to control the sensitivity for the remote control signal while not affecting sensitivity for audio frequency induction signals. This reduces audible interference from the remote control.

In a further aspect of the invention, a computer interface permits programming hearing aids or remote controls that uses a computer parallel port to supply power for the interface and to provide bidirectional communication. This eliminates the size, cost, and inconvenience of a separate power supply. The computer software is able to control the signal switching pattern. Such a computer interface makes it possible to program hearing aids or remote controls by use of a transformer to transmit power to the interface and optocouplers to transmit signals to and from the interface. This provides electrical isolation needed to meet safety requirements.

A hearing aid embodying the present invention can incorporate a signal-processing algorithm in which numerous parameters are field programmable over selected ranges in each of two channels. These include:
Full-on Gain: 48 dB range in 3 dB increments.
Corner Frequency: 500, 707, 1000, 1414, 2000, 2828, or 4000 Hz. Phase: In phase or out of phase.
Primary Output AGC System

Limiting Level: 48 dB range in 3 dB increments.
Release Time: 2 to 8192 msec in powers of 2.

Secondary Output AGC System

Limiting Level: 48 dB range in 3 dB increments.
Release Time: 2 to 8192 msec in powers of 2.

Primary Input AGC System

Threshold Level: 48 dB range in 3 dB increments.
Compression Ratio: 1.14, 1.33, 1.6, 2.67, 4, or 8.
Attack Time: 2 to 8192 msec in powers of 2.
Release Time: 2 to 8192 msec in powers of 2.

Secondary Input AGC System

Threshold Level: 48 dB range in 3 dB increments.
Compression Ratio: 1.14, 1.33, 1.6, 2.67, 4, or 8.
Attack Time: 2 to 8192 msec in powers of 2.
Release Time: 2 to 8192 msec in powers of 2.

Noise Reduction System

Threshold Level: 48 dB range in 3 dB increments.
Attack Time: 2 to 8192 msec in powers of 2.

The following parameters may be programmed at the time of hearing aid manufacture over various ranges in each of two channels.

Primary Output AGC System

Attack Time: 2 to 8192 msec in powers of 2.
Secondary Output AGC System
Attack Time: 2 to 8192 msec in powers of 2.
Noise Reduction System
Release Time: 2 to 8192 msec in powers of 2.

A fitting system can be provided that uses a fitting algorithm to select hearing aid parameters based on the factors of abnormal growth of loudness, widening of critical bands, abnormal upward spread of masking, and binaural vs. monaural fitting.

Reference will now be made, by way of example, to the accompanying drawings, in which:-

Fig. 1 is an overall diagram of a system in accordance with the present invention;
Fig. 2 is a block diagram of a digital hearing aid in accordance with the present invention;
Fig. 3 is a block diagram of an electronic system usable with the hearing aid of Fig. 2;
Fig. 4 is block diagram of an analog-to--digital converter in accordance with the present invention;
Fig. 5 is a block diagram of a digital signal processor for the audio signal path in accordance.with the present invention;
Fig. 6 is a block diagram of a digital-to--analog converter in accordance with the present invention;
Fig. 7 is a block diagram of a control unit in accordance with the present invention;
Fig. 8 is a block diagram of an interface system in accordance with the present invention;
Fig. 9 is a block diagram of a remote control unit in accordance with the present invention;
Fig. 10A is a block diagram of a wired programming interface in accordance with the present invention; and
Fig. 10B is a block diagram of a wireless programming interface in accordance with the present invention.

While this invention is susceptible of embodiment in many different forms, there is shown in the drawings and will be described herein in detail, specific embodiments thereof with the understanding that the present disclosure is to be considered as an exemplification of the principles of the invention and is not intended to limit the invention to the specific embodiments illustrated.

A digital hearing aid system 10 of Fig. 1 contains digital hearing aids 12, 14 (binaural fitting) or a single digital hearing aid 12 or 14 (monaural fitting) worn by the user. The hearing aids 12, 14 are optionally equipped with programming sockets 12a, 14a to allow the hearing aid characteristics to be programmed for the individual user.

A remote control unit 16 is carried by the user to control the operation of the hearing aid(s) 12, 14. The unit 16 is capable of transmitting, via radiant electromagnetic energy R, user-selected commands and parameter sets to the hearing aid(s) 12, 14 to adjust the hearing aids characteristics for various listening environments. The remote control unit 16 is equipped with a programming socket 16a to allow entering and storing of a number of user-selectable programs or parameter values.

A programming interface 18 is coupled to a personal computer 18a. Programming cords and plugs 18b, 18c transmit the electrical signals needed to program the hearing aid(s) 12, 14 and remote control unit 16.

Alternately, the hearing aids 12, 14 are equipped with a wireless transmitter 18d and receiver 18e. The hearing aids 12, 14 can thus be remotely programmed or controlled. In addition, pickup 18e' can detect previously stored programs or data being read back to receiver 18e.

A fitting program 18f can be run on the personal computer 18a to accept audiological data for the user, to determine the appropriate characteristics of the hearing aid(s) 12, 14 for that user, and to provide the appropriate data to the programming interface 18. The fitting program 18f can also provide other functions, such as storage and retrieval of user - specific data.

The hearing aid system 10 may be provided in various forms. For example, the hearing aid(s) 12, 14 may be behind-the-ear (BTE), in-the-ear (ITE), or in - the-canal type. Also the system 10 may be configured without the remote control unit 16, using a limited set of hearing aid mounted controls instead. The system 10 may even be configured with no user operated control other than an on/off switch.

Fig. 2 illustrates a block diagram for a hearing aid such as the aid(s) 12, 14.

The digital hearing aid(s) 12, 14 of Fig. 2 each contain a microphone 20 to receive acoustic signals in the audio frequency band. An inductive pickup coil 22 serves multiple a dual purposes.

The coil 22 receives magnetic field signals in the audio frequency band from a telephone receiver or a transmitting induction loop. It can also receive remote control signals encoded on a transmitted or radiated electromagnetic carrier whose frequency is above the audio band. It can also be used to receive programming signals from transmitter 18d or to transmit programs or information to receiver 18e. For a hearing aid without an induction pickup option and without remote control and wireless options, the induction coil 22 is not needed.

The connector 12a can optionally be provided for bidirectional transfer of encoded programming signals. Transfer can be in serial or parallel.

An electronic signal processor 24 receives the above signals together with control signals from optional hearing aid mounted controls 26 and provides an electrical output signal at an output port 24a. A receiver 28 converts this electrical output signal to an acoustic output signal.

A battery provides power for the electronic signal processor 24.

The electronic signal processor 24 is illustrated in block diagram form in Fig. 3. The following table further explains the nature of the signals S1 to S21 shown in Figure 3.

S1	Analog - audio freq.
S2	1 bit 400 KHz
S3	13 bits 400 KHz
S4	2 bits 400 KHz
S5	2 line output, audio with 400 KHz carrier
S6	analog - audio freq.

S7 control signals
S8 analog
S9 analog
S10 modulated 50 KHz carrier
S11 1 bit digital serial data
S12 control lines
S13 address; data; control
S14 address; data; control
S15 data 24 bits
S16 address bits
S17 8 bit data
S18 address bits
S19 9 bits parallel two interleved 12.5 Kbit signals
S20 10 bits control signals
S21 9 bits parallel two interleaved 12.5 Kbit rate signals

The processor 24 contains an induction coil preamplifier 22a to amplify the audio frequency signals and the remote control signals detected by the induction coil 22. Automatic gain control (AGC), is included to control the output level of the remote control signal.

A remote control signal detector 22b is coupled to the preamplifier 22a to recover the modulating signal from the carrier signal detected by coil 22.

A preamplifier 20a is provided to amplify the signal from the microphone 20 and/or the output signal from the induction coil preamplifier 22a. AGC limiting is included to prevent overloading by high input signal levels.

An analog-to-digital converter 30 is provided to convert the analog output of the preamplifier 20a to a digital form. The A/D converter 30 is based on sigma-delta modulation of the type described in Oversampling Delta-Sigma Data Converters, Candy and Temes Ed., IEEE Press 1992.

A digital signal processor 32 for the audio path is provided to process the signals received from the A/D converter 30. The signals are split into low and high frequency bands or channels with adjustable corner frequencies in the processor 32. The gain, phase, and corner frequency of each channel are controlled by signals from a control processor 34. The signals from the two channels are then recombined.

A digital-to-analog converter 36 is provided to convert the digital output signal stream from the audio signal processor 32 into a bit stream from which analog information, corresponding to the original acoustic input, can be recovered by low-pass filtering. This filtering occurs in the output transducer 28, the receiver for the aid 12.

An output driver 36a drives the output transducer 28 (a magnetic receiver for example) in a switching type configuration. This arrangement provides high power conversion efficiency.

The digital signal processor 34 for the control path 34 receives signals from the outputs of the two frequency channels of the audio signal processor 32 (best seen in Fig. 5) and produces control signals to provide real-time control of the gain of each channel. It also provides signals to control the corner frequency and phase of each channel.

An instruction memory 34a coupled to the processor 34 provides instructions to the processor 34 to implement a control method. It will be understood that one of the advantages of the signal processor of Fig. 3 is that different control methods can be provided for different hearing deficiencies. Further, the method can be altered over time to take into account changes in a particular deficiency.

Instructions can be loaded into the instruction memory 34 at the time of manufacture, or later if desired, via an interface processor 38. The memory 34a could be a non-volatile semiconductor memory.

A parameter memory 34b provides control parameters to the control processor 34 to tailor the hearing aid characteristics to the hearing loss and needs of the hearing aid user. The parameter memory 34b preferably includes a volatile memory and a shadow non-volatile memory.

Parameters may be loaded into the parameter memory 34b via the remote control unit 16, the wireless programmer 18 or the programming connector, such as connector 12a, and may be read from the parameter memory 34b via the wireless interface of the programming connector. Parameters can be transferred from the non-volatile portion of parameter memory 34b to the volatile portion when the hearing aid is turned on and may be transferred back and forth between these two memory types via commands from the remote control 16, the transmitter 18d or programming connector such as connector 12a. The parameter memory 34b also stores hearing aid identification data.

A working memory 34c provides temporary storage for the working variables of the control processor 34.

The interface processor 38 controls parallel or serial transmission or reception via input/output devices. These include the programming connector 12a or the remote control coil 22. When transmitting, serial data, for example, is provided, at connector 12a. Simultaneously the same signal is modulated and coupled to the coil 22'.

The processor 38 also receives inputs from optional hearing aid mounted controls. The processor 38 provides control signals to the preamplifier 20a for selection of microphone and/or induction coil inputs.

In addition various support functions are provided, such as voltage regulation, clock generation, and power-down functions. These functions are all a type well known to those of skill in the art and as a result are not addressed further.

The electronic signal processor 24 can be partitioned into functions that are primarily analog and functions that are primarily digital in nature, as illustrated in Figure 3. The analog and digital functions can be integrated on separate chips to minimize the effects of digital noise on low level analog functions.

The A/D converter 30 illustrated in block diagram form in Fig. 4 contains an analog summer 30-1 to add the analog input signal on the line 20b and an inverted feedback signal on a line 20c, producing an error signal on a line 30-2. First, second, and third analog integrators 30-3 to 30-5, in tandem, successively integrate the error signal. A feedback path 30-6 from the output of the third integrator 30-5 to the input of the second integrator 30-4 produces a zero in the transfer function at about 6000 Hz.

A coefficient combiner 30-7 that provides a weighted sum of the analog outputs of the three integrators 30-3 to 30-5, provides a frequency weighted representation of the error signal. An analog clipping amplifier 30-8 amplifies the combined signal to a suitable level.

A comparator 30-9 converts the amplified signal to a two-level (on/off) signal. A state detector 30-10 samples and latches the state of the comparator output at integer intervals of a clock (such as a 400 kHz rate). The output of the state detector 30-10 is the digital output of the A/D converter on a line 30-11.

A pulse generator 30-12, produces a digital feedback signal consisting of a short pulse when the digital output is a logic zero and a long pulse when the digital output is a logic one. A one-bit D/A converter 30-13 inverts the digital feedback signal and converts it to an analog feedback on the line 20c with controlled signal levels.

The audio signal processor 32 is illustrated in block diagram form in Figure 5. It contains a decimation stage 32-1 with a decimation filter and a decimeter that discards excess samples. For decimation by 2, the transfer function of the decimation filter is

$$(1+Z^{-3})\,(1+Z^{-1})\,(1+Z^{-1})/8$$

and every other sample is discarded, reducing a 400 kHz sample rate to 200 kHz.

The audio signal processor 32 may be implemented without a decimation stage, but then subsequent digital filter stages must operate at twice the sample rate, reducing the possibilities of multiplexing filter elements.

A band splitter and gain multiplier 32-2 multiplies the digital input by low-channel gain and phase values to provide an input to a low frequency channel filter 32-3, and multiplies the digital input by high-channel gain and phase values to provide the input to a high frequency channel filter 32-4.

The high-channel filter 32-4 includes the following stages in series:

A first-order low-pass digital filter 32-5 with a corner frequency of 4000 Hz. This filter is implemented with adders and clocked registers and is multiplexed with a first order filter 32-6 in the low channel.

A second-order high-pass digital filter 32-7 with a Q of .707 has a programmable corner frequency. This filter is implemented with multiplexed adders and clocked registers.

A second-order low-pass digital filter 32-8 with a Q of 1.414 has a corner frequency of 5656 Hz. The purpose of this filter is to reduce the level of high frequency quantization noise. It is implemented with multiplexed adders and clocked registers.

The low channel filter 32-3 includes the following stages in series:

The first-order high-pass digital filter 32-6 with a corner frequency of 125 Hz. This filter is multiplexed with the first-order filter 32-5 in the high channel 32-4.

A second-order low-pass digital filter 32-9 with a Q of .707 and a programmable corner frequency. This filter is implemented with multiplexed adders and clocked registers.

A sum and limit stage 32-10 limits the signal range of the digital inputs from the high and low channels, adds them, and then again limits the range of the summed signal on a line 32 -11. The result is the output signal from the audio signal processor 32.

A decimetor 32-12 decimates the outputs of both the high channel filter 32-4 and the low channel filter 32-3 by a factor of 16 to a sample rate of 12,500 samples/sec. Each decimation filter consists of a 16 sample sum and dump (sinc filter). The resulting high and low channel output signals are time multiplexed onto a single output bus 34-5.

The D/A converter 36 is illustrated in Fig. 6. It includes an adder 36-1 that combines the digital input signal on the line 32-11 with an inverted two-valued digital feedback signal on a line 36-2 to produce an error signal on a line 36-3.

First, second, and third accumulators or registers 36-4 to 36-6 in series, successively accumulate the error signal.

An adder 36-7 is provided between the first and second accumulators 36-4 and 36-5 for injecting a feedback signal from the third accumulator 36-6 to introduce a transfer function zero at 5.6 kHz.

An adder 36-8 provides a weighted sum of the digital outputs of the three accumulators 36-4 to 36-6, providing a frequency weighted representation of the error signal.

A quantizer 36-9 provides a two-valued (one - bit) digital output from the multi-bit frequency weighted error signal on a line 36-9'. This is the first output of the D/A converter.

An inverter 36-10 receives the first output and produces a second, inverted, output of the A/D converter on a line 36-11.

The control processor 34 is illustrated in Fig. 7. It contains an instruction decoder 34-1 that receives instructions from the instruction memory 34a and status signals from various elements in the control processor. It provides signals to control the operation of the various processing elements and input and output selectors as well as to control read operations from the parameter memory 34b. It also controls read and write operations

to the variable memory 34c.

A program counter 34-2 controls the sequencing of instructions from the instruction memory 34a. A pair of general purpose counters 34-3 are available to be loaded, decremented, and tested by software.

A pseudo-logarithmic converter 34-6 produces a piecewise linear approximation to the negative of log (base2) of the absolute value of the input. This operation produces a time multiplexed logarithmic representation of the signal magnitudes in the two channels 32-3 and 32-4.

A pseudo-exponential converter 34-8 produces a piecewise linear approximation of exp(base 2) of the negative of the input. This converts the time multiplexed logarithmic representation of the gain control signals to linear domain gain multipliers for the two channels 32-3 and 32-4.

A multiplier 34-10 is present in a first or in the "A" operand path 34-12 of the control processor 34. It multiplies the A input from "A" selector gates 34-14 by a 3 bit multiplicand or by the value 1 received from "M" selector gates 34-15.

A barrel shifter 34-16 is located in the "A" operand path 34-12 after the multiplier 34-10. The shifter 34-16 left shifts the"A"operand 0 to 15 bit positions in response to a control input from shift selector gates 34-17.

An arithmetic and logic unit (ALU) 34-18 receives an "A." operand from the barrel shifter 34-16 and a "B" operand from a "B" input selector circuit 34-19. It performs the operations of addition (A+B), subtraction (A-B), and tests for the conditions Result=zero and Result<zero.

A conditional selector circuit 34-22 is coupled to the output of ALU 34-18. The selector, which could be implemented with combinational gating, selects either the output of the ALU 34-18 or, in response to conditional select command from the "B" selector gating 34-19,selects either the "A" operand or the "B" operand depending on the Result <0 output of the ALU.

An accumulator 34-23 stores the output of the conditional selector 34-22 for one instruction cycle. A condition register 34-25 stores the condition test results of the ALU 34-18 for one instruction cycle.

The "A" selector circuitry 34-14 for the "A" operand selects one of the following: a parameter obtained from the parameter memory 34b, the output of the accumulator 34-23, the magnitude signal from the high 32-4 or low 32-3 channel or an immediate operand from the instruction word from the instruction memory 34a. The "A" selector 34-14 supplies the first input to the multiplier 34-10.

The "M" selector circuitry 34-15, the second input to the multiplier 34-10, selects either a parameter obtained from the parameter memory 34b, an immediate operand from the instruction word from the memory 34a or a multiplier of 1.

The "S" selector circuitry 34-17 for the shift input of the barrel shifter 34-16 selects either a parameter obtained from the parameter memory 34b or an immediate operand obtained from the instruction from the memory 34a or a zero shift command.

The "B" selector circuitry 34-19 for the "B" operand selects either a variable obtained from the variable memory 34c, the output of the accumulator 34-23, the volume control signal on a line 34-27 or an immediate operand obtained from the instruction word from the memory 34a.

A frequency register 34-29 latches the channel frequency and phase parameters when the first two parameter addresses are accessed.

The interface processor 38 is illustrated in block diagram form in Fig. 8. It contains a pulse conditioner 38-1 that receives a signal stream from the remote control unit 16 via the remote signal detector coil 22'. The conditioner 38-1 provides envelope detection of this signal stream while also correcting for short spikes and drop outs.

An input detector circuit 38-2 monitors incoming data from both the pulse conditioner 38-1 and the programming connector 12a. The detector waits for the presence of a conditioning pulse. When a conditioning pulse is received, the input detector 38-2 generates a control signal indicating that valid data is arriving. When the end of transmission is detected, the control signal is reset.

A serial/parallel converter 38-3 shifts incoming serial data into a register and outputs 8-bit parallel data to a parallel data bus 38-5 at appropriate times. The serial/parallel converter 38-3 is also used to convert 8-bit parallel data to serial data when data is to be output to the programming connector 12a.

A clock/bit-counter 38-6 controls the shifting of serial data in the serial/parallel converter 38-3 and times the transfer of parallel data to or from the parallel data bus 38-5.

A parity check circuit 38-6' checks the parity of incoming data and generates an error signal if a parity error occurs. The parity check circuit 38-6' also provides the correct parity bit for data transmitted from the hearing aid 12, 14.

A coder circuit 38-7 provides a serial output data stream to programming connector 12a and to coil 22'. The coder 38-7 produces a short pulse for each zero bit to be transmitted out to the programming connector 12a and a long pulse for each one bit.

A modulator 38-8 receives the data signals from coder circuit 38-7 and uses those signals to modulate a 50kHz carrier. This modulated signal is used to drive the tuned coil 22' providing wireless transmission.

An antenna switch 38-9 switches coil 22' between receive and transmit modes. In the receive mode it is coupled to the coil preamplifier 22a. In the transmit mode it is disconnected from that preamplifier and coupled to the modulator 38-8.

An ID control circuit 38-10 compares the first byte of an incoming transmission (the ID byte) to a stored ID byte identifier. If the ID bytes do not match, a signal is

given to reset the serial interface and ignore the following transmission.

A command latch 38-12 latches the second byte of an incoming transmission (the command byte). The command byte consists of the following command bits:

PWDN command to power-down the hearing aid to conserve power when not in active use.

VUP command to increase the volume setting of the hearing aid.

VDN command to decrease the volume setting of the hearing aid.

RD command to read out, by subsequent bytes sent out via the serial port, the parameters representing the current settings of the hearing aid.

WRT command to write to the hearing aid, by subsequent bytes sent in via the serial port, the parameters representing a new setting of the hearing aid.

RCL command to recall parameters from the non-volatile portion of the parameter memory to the working portion, making these parameters the current setting of the hearing aid.

STO command to store the parameters in the working portion of the parameter memory to the non-volatile portion.

PRG command to select stored control program A or control program B.

A byte counter 38-14 identifies the incoming byte sequence and generates addresses for memory accesses. An interface control circuit 38-16 controls the operation of other elements in response to the commands that have been received.

A microphone/telephone circuit 38-18 controls microphone or telephone coil selection based on commands received from the remote control or inputs from an optional hearing aid mounted M/T switch. It also controls a power-down function when a power-down command is received or if neither microphone nor telephone are selected.

A volume control module 38-20 provides volume control setting information based on commands received from the remote control or from an optional hearing aid mounted volume control.

A program select circuit 38-22 permits the selection of either pre-stored control program A or program B. This selection is in response to commands received from the connector, such as 12a or the coil 22'. Alternately, an optional switch mounted on the housing of the hearing aid 12, 14 can be used to select one of the pre-stored programs.

With respect to Fig. 9, the remote control unit 16 includes the following elements:

a microcontroller 60 containing a microprocessor, program memory, data memory, timer, and input/output ports;

a serial EEPROM unit 62 connected to the microcontroller 60 for storage and retrieval of parameter sets (hearing aid programs and identification data);

a keyboard 60a for entry of commands to the microcontroller; an LED display 60b driven by the microcontroller to indicate data transmission and battery status;

drivers 64a, 64b connected to output ports of the microcontroller 60 to drive transmitting coils in phase quadrature with high efficiency;

two tuned transmitting coils 66a, 66b, in orthogonal orientation, driven in phase quadrature by drivers 64a, 64b;

a programming port 68 provided for bidirectional serial communication with the programming interface 18 - the port 68 includes the connector 16a, and voltage translators 68a to convert voltage levels between the programming port and the microcontroller;

a battery 70a provided to power the electronics; and

a low-voltage detector 70b for sensing when the battery is nearing the end of its life.

The programming interface 18 provides for data transmission between a computer and a hearing aid or remote control unit. Fig. 10A is a block diagram of an interface 80 with programming plugs 18b, 18c. Fig. 10B is a block diagram of a wireless interface 82.

In the interface 80, a connector 80a mates with the parallel port of the personal computer 18a. That also allows a parallel data device such as a printer to be connected to the parallel port. Control logic 80b senses when the parallel port is to control the parallel data device and when it is to control the programming interface. The control logic also senses when data is being sent out by the computer 18a and when data is to be received and selects the proper signal path.

The system for transmission or reception via programming cable of data to or from a hearing aid or remote control unit contains opto-isolators 84a, 84b and voltage translators 86a, 86b for converting between the voltage levels of the programming port and the control logic levels.

One or more programming connectors 18b, 18c each having a bidirectional data line, a ground line, a supply voltage line connected to an isolated voltage supply or a battery.

Alternately, when only a small amount of power is needed, the power supply can be derived by drawing power from the data lines of the parallel port. A circuit 88 for providing isolated supply voltage includes an oscillator 88a, a transformer 88b, a rectifier 88c, and a voltage regulator 88d.

The system 82 for wireless transmission of commands and programs to the hearing aid, contains the following elements:

a carrier oscillator 92, gated by a signal from control

logic 92a, which produces two modulated carriers in phase quadrature to high efficiency driver 94a, 94b; and
drivers 94a, 94b which drive tuned transmitting coils 96a, 96b in orthogonal orientation.

A system for wireless reception of data from the hearing aid contains the following elements:

a tuned receive coil 98a - the coil 98a may be connected by cable to allow it to be brought near to hearing aids while they are worn; and
an amplifier 98b and detector 98c coupled to the received signal for providing a demodulated signal to the control logic 92a.

From the foregoing, it will be observed that numerous variations and modifications may be effected without departing from the spirit and scope of the invention. It is to be understood that no limitation with respect to the specific apparatus illustrated herein is intended or should be inferred. It is, of course, intended to cover by the appended claims all such modifications as fall within the scope of the claims.

Claims

1. A hearing aid, having alterable parameters, comprising:

   analog-to-digital input circuitry (30) for forming a digital signal representative of an incident acoustic wave;
   a digital signal processor (32), coupled to said input circuitry (30), wherein said processor forms and processes first and second, frequency distinguishable, data streams representative, at least in part, of said digital signal, at a first rate;
   a control unit (34), coupled to said processor (32), wherein said unit (34) includes circuitry for logarithmically processing at least one of said digital data streams, at a reduced rate, less than said first rate;
   parameter value storage memory (34b) coupled to said unit; and
   an interface (38) for accessing said memory (34b) and altering parametric values stored therein.

2. An aid as claimed in claim 1, wherein said control unit includes decimation circuitry.

3. An aid as claimed in claim 1, wherein said processor (32) includes first and second digital filters (32-3, 32-4).

4. An aid as claimed in claim 3, wherein said control unit interacts with and converts said data streams to logarithmic representations of said digital signal.

5. An aid as claimed in claim 3, wherein said processor includes combining circuitry for forming a single, output, digitized, data stream representative of said digital signal.

6. An aid as claimed in claim 1, wherein said interface (38) includes a receiver of remotely generated wireless signals.

7. An aid as claimed in claim 6, wherein said interface (38) further includes a transmitter of wireless signals.

8. An aid as claimed in claim 1, wherein said interface (38) is accessible by transmitted radiant energy.

9. An aid as claimed in claim 1, wherein said control unit includes an instruction storage memory.

10. An aid as claimed in claim 1, wherein said processor includes first and second, parallel, digital filters wherein each said filter has a plurality of parameters associated therewith and wherein at least some of said parameters are remotely alterable via said interface.

Fig. 1

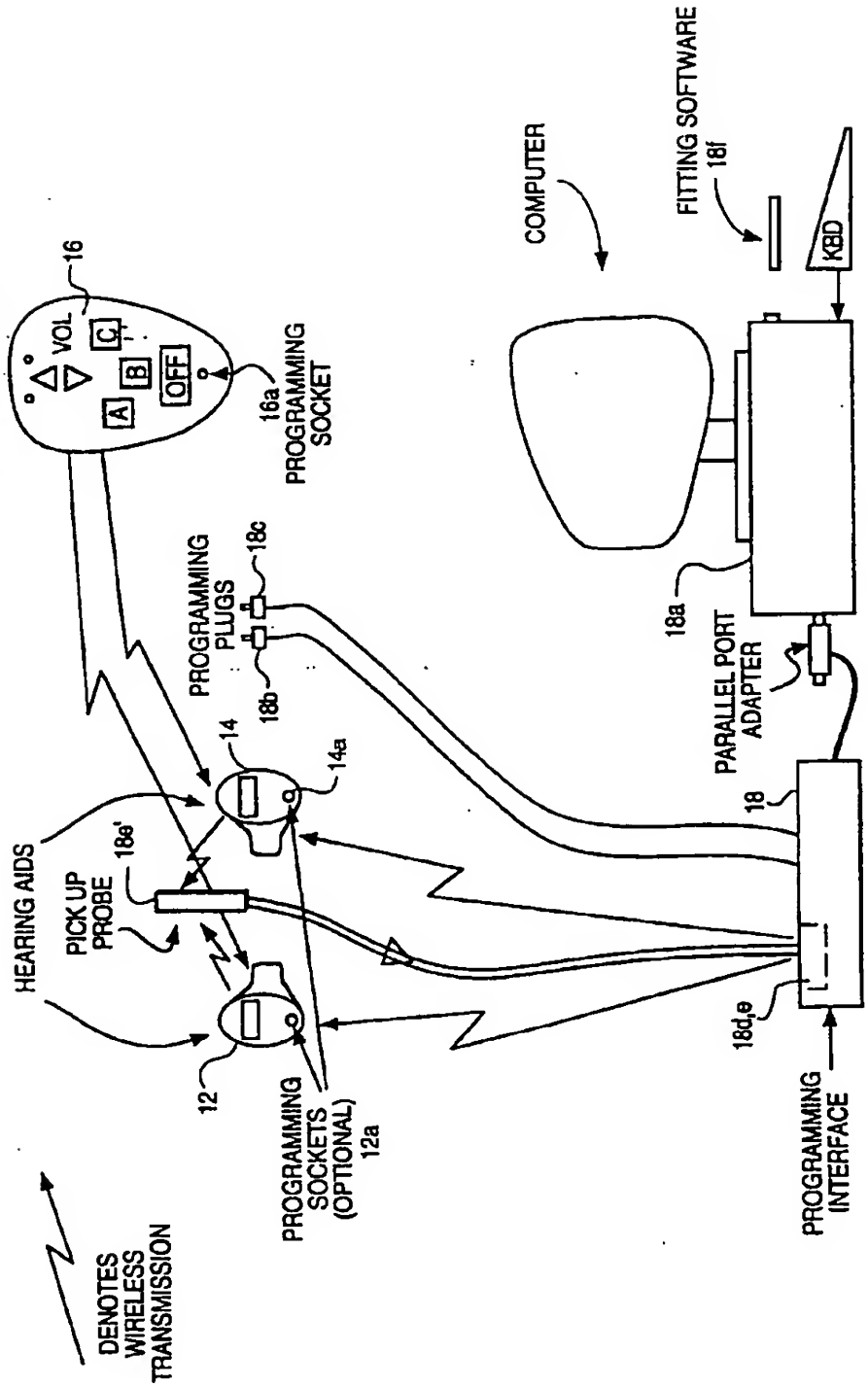
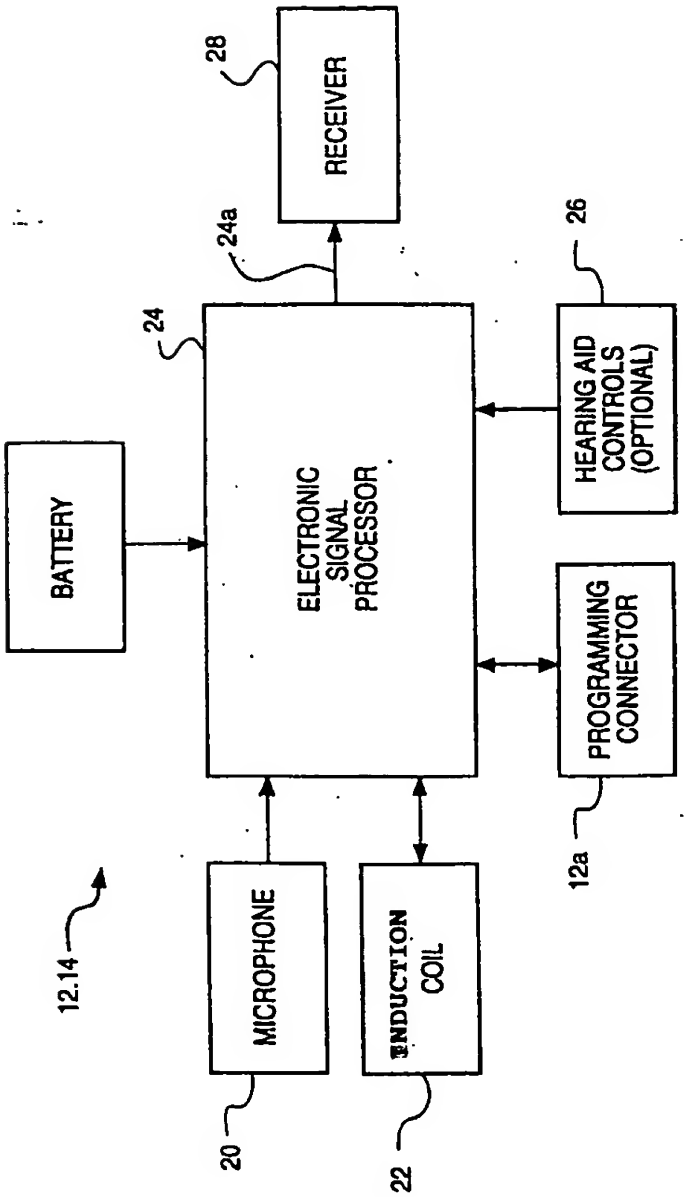


Fig. 2



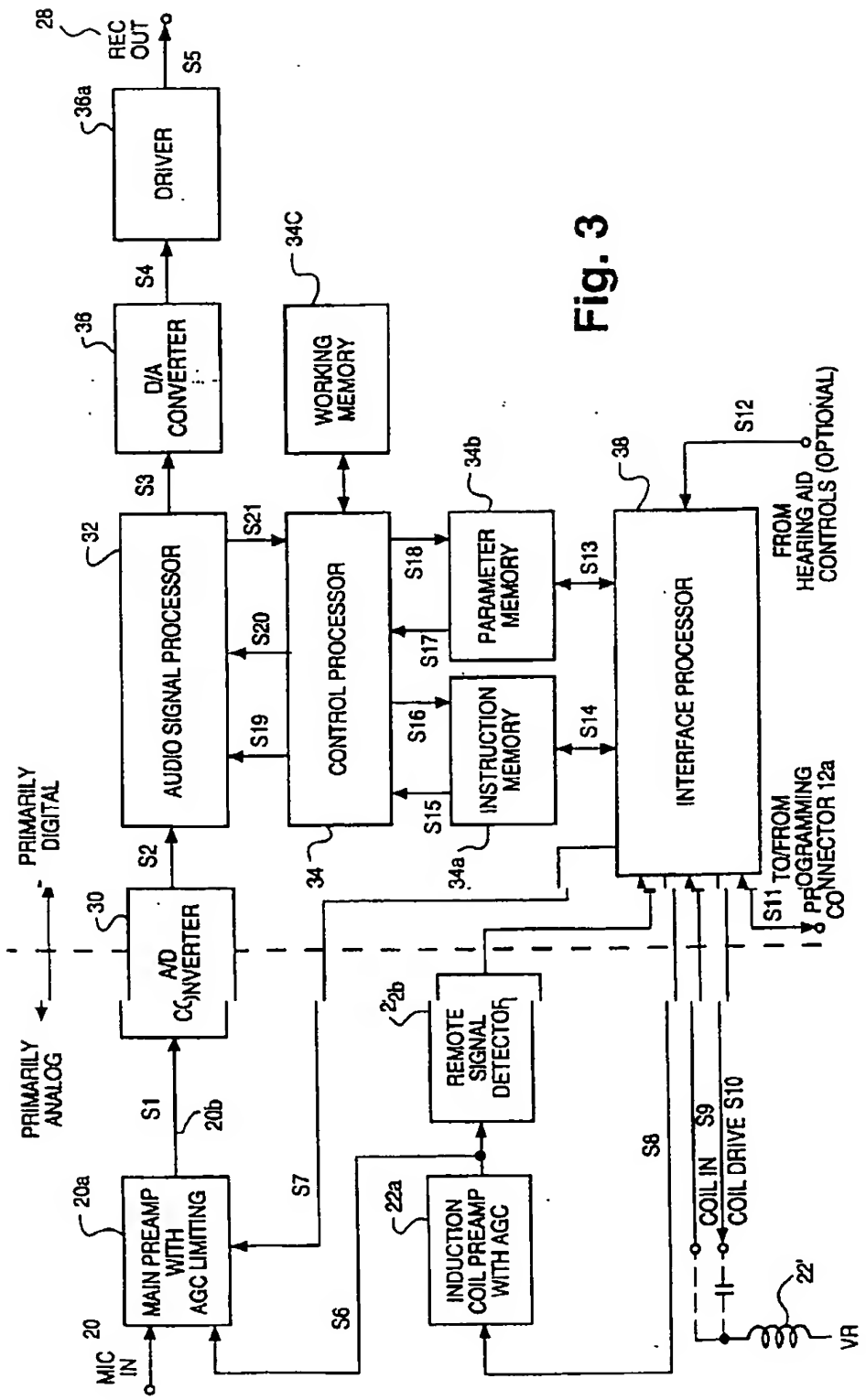
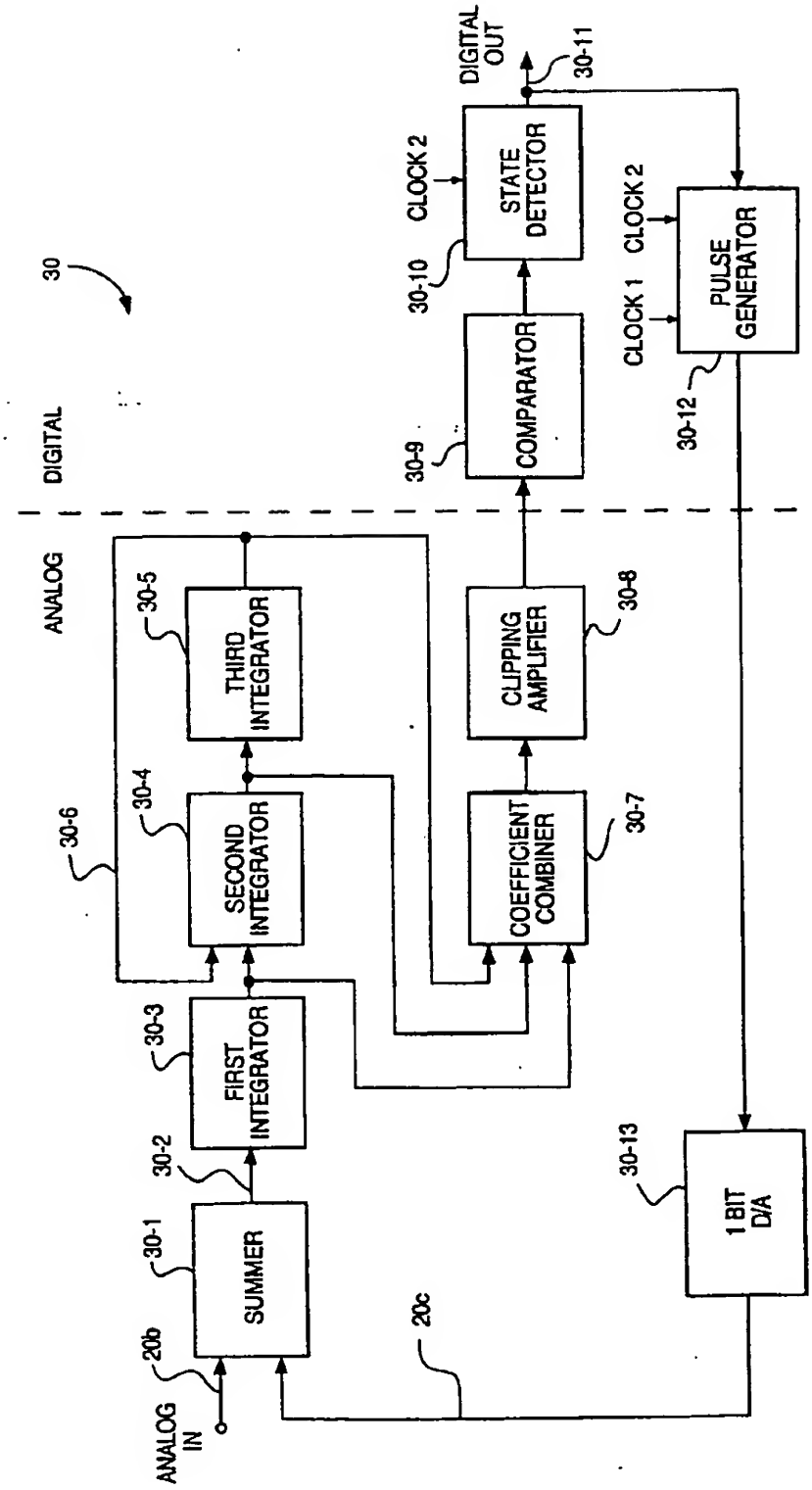


Fig. 3

Fig. 4



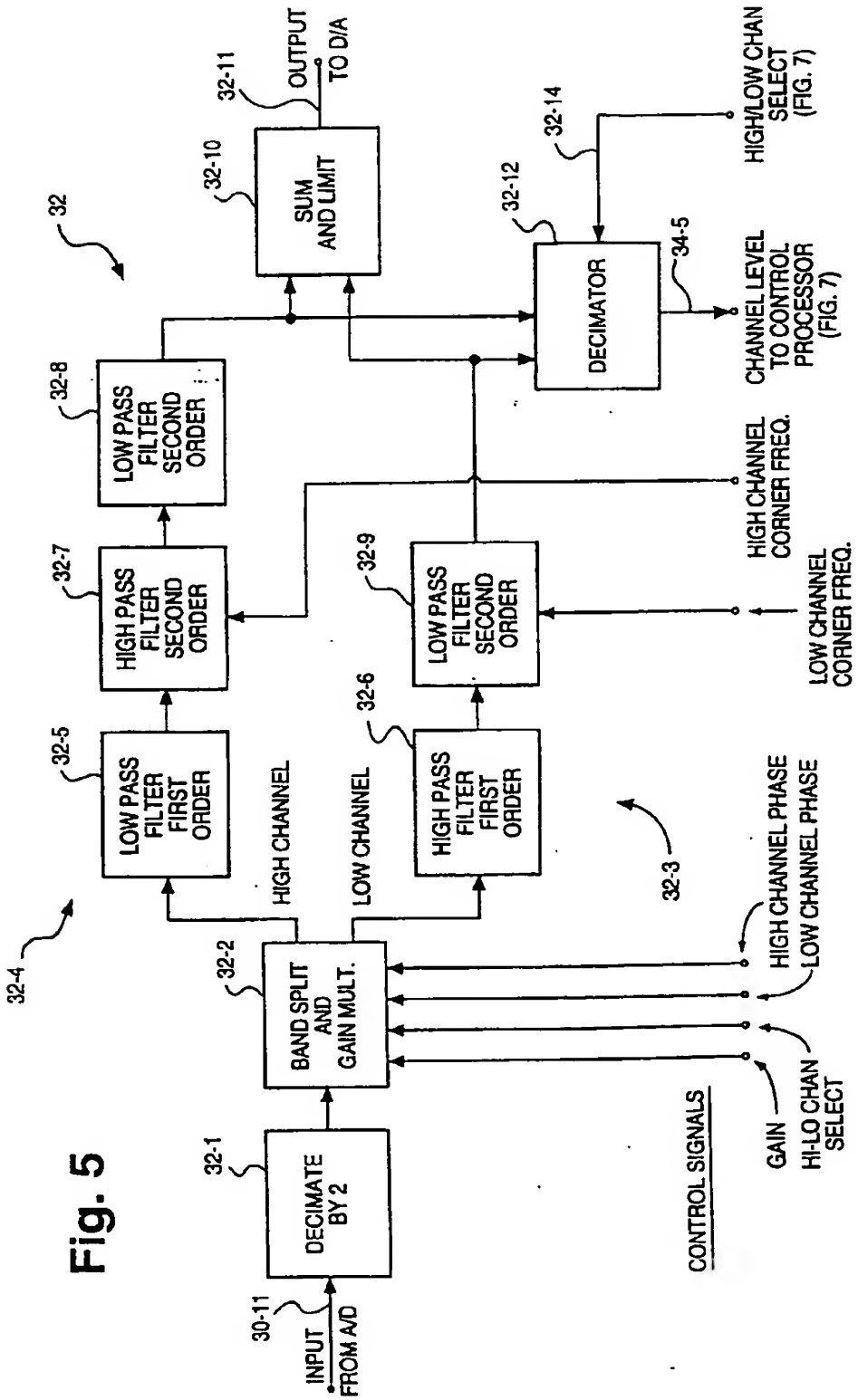


Fig. 5

Fig. 6

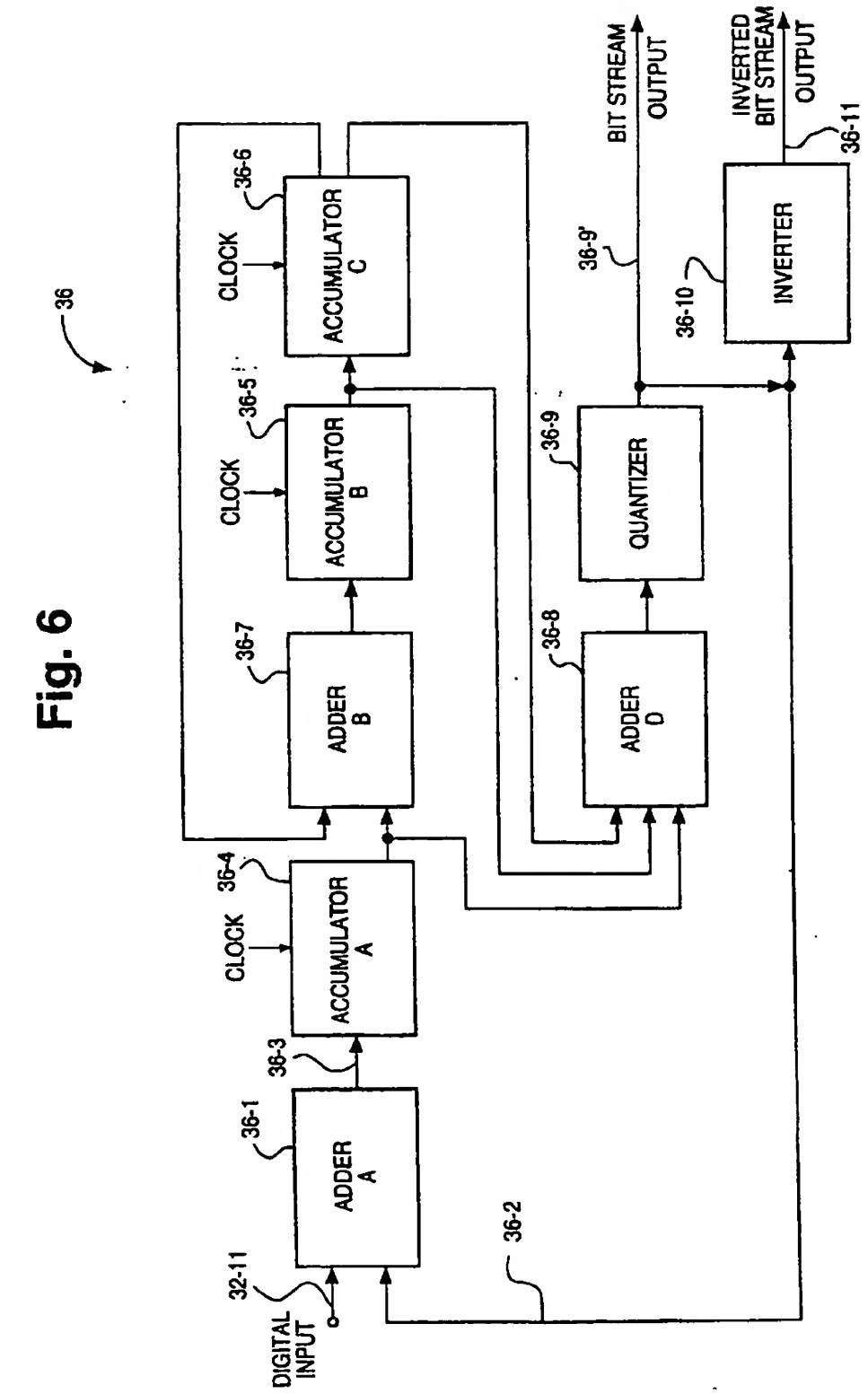


Fig. 7

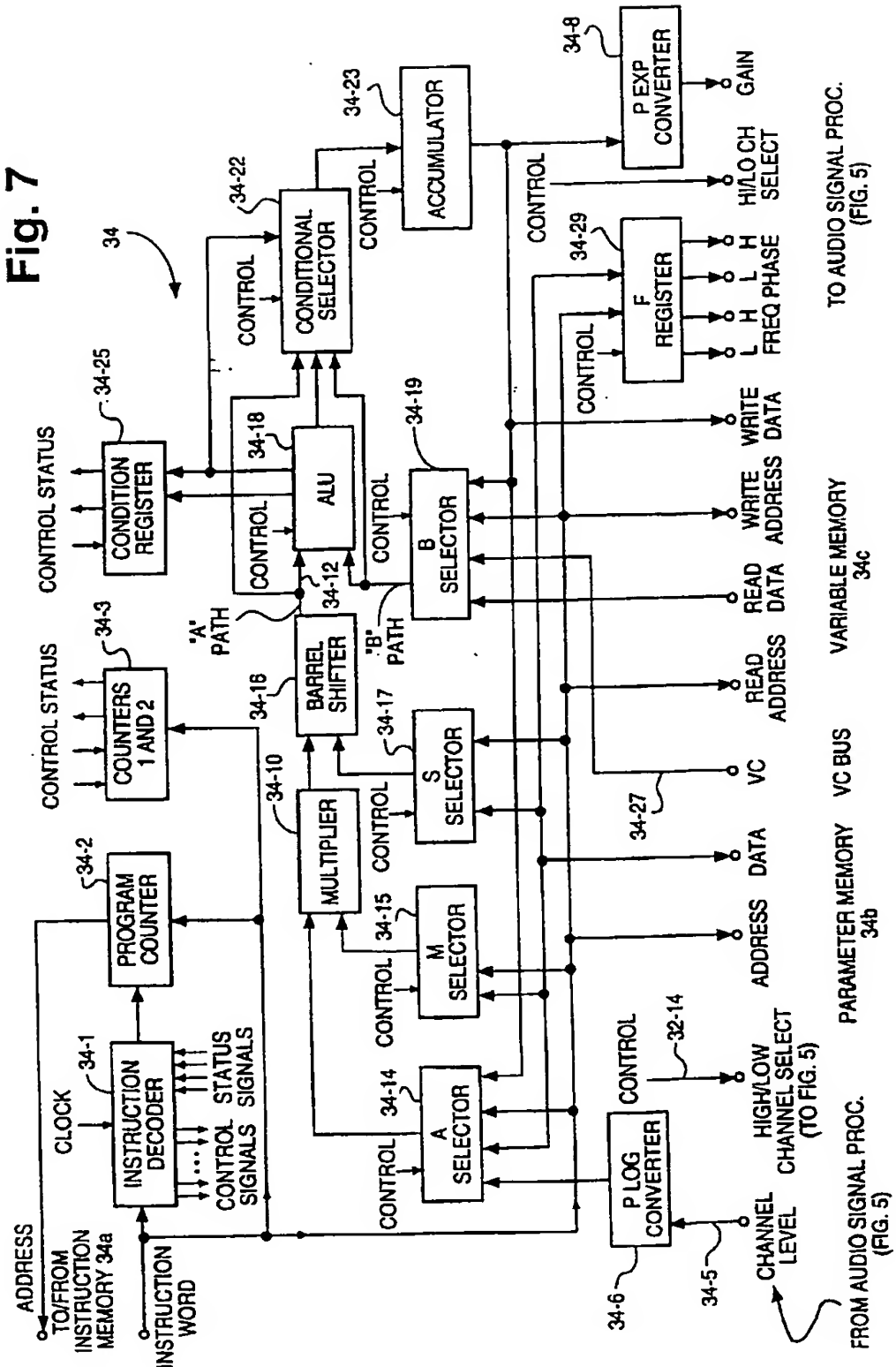


Fig. 8

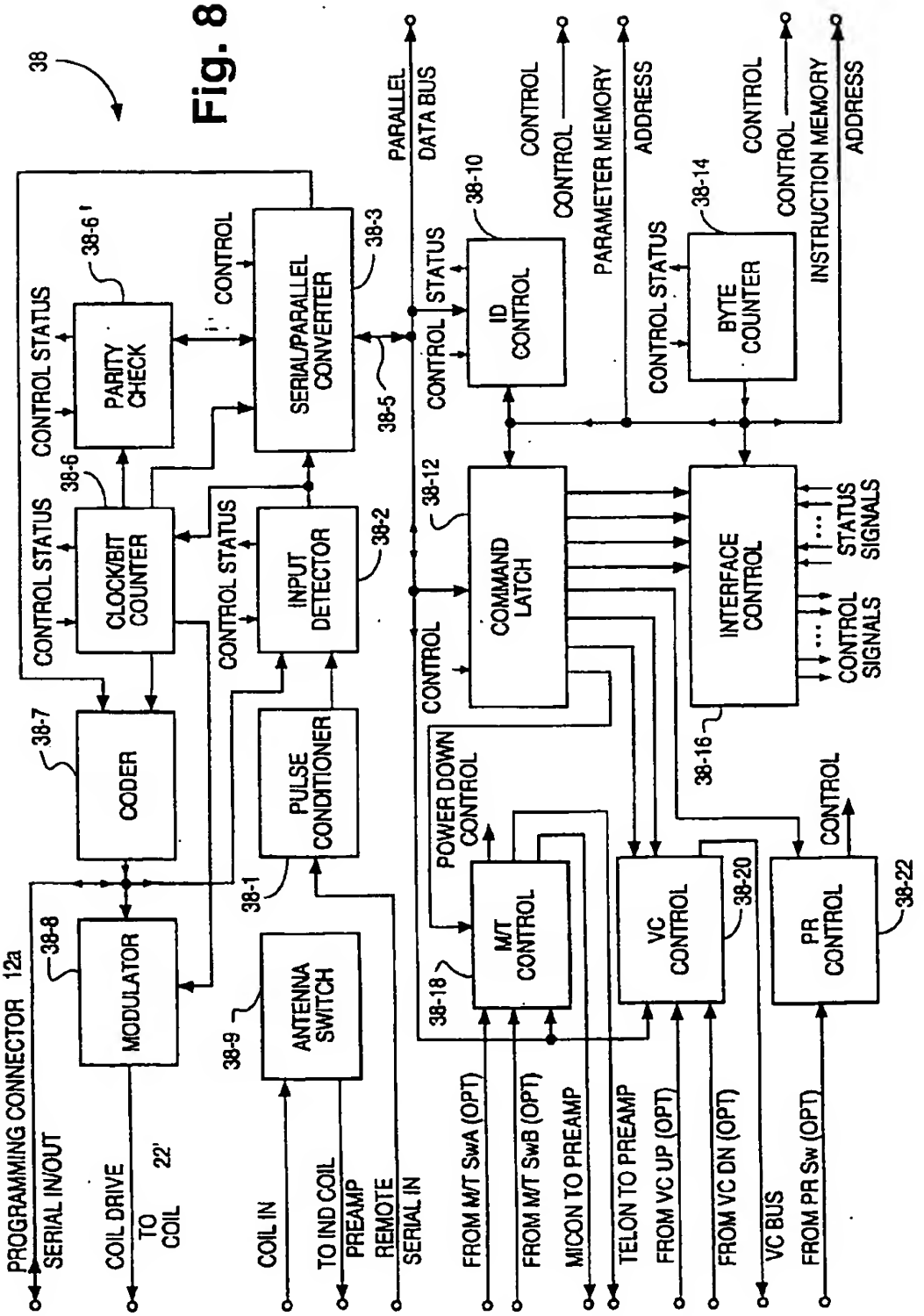


Fig. 9

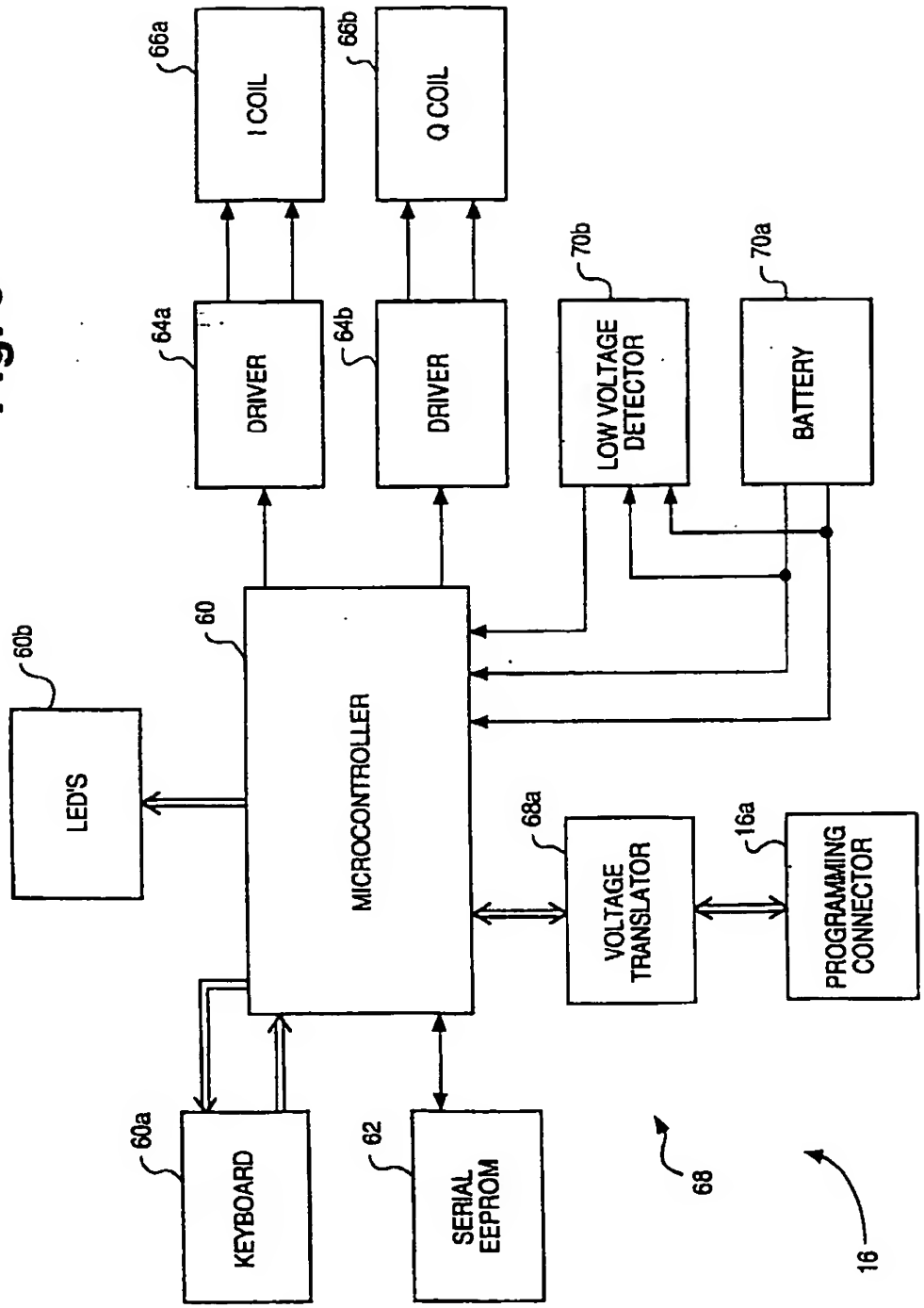
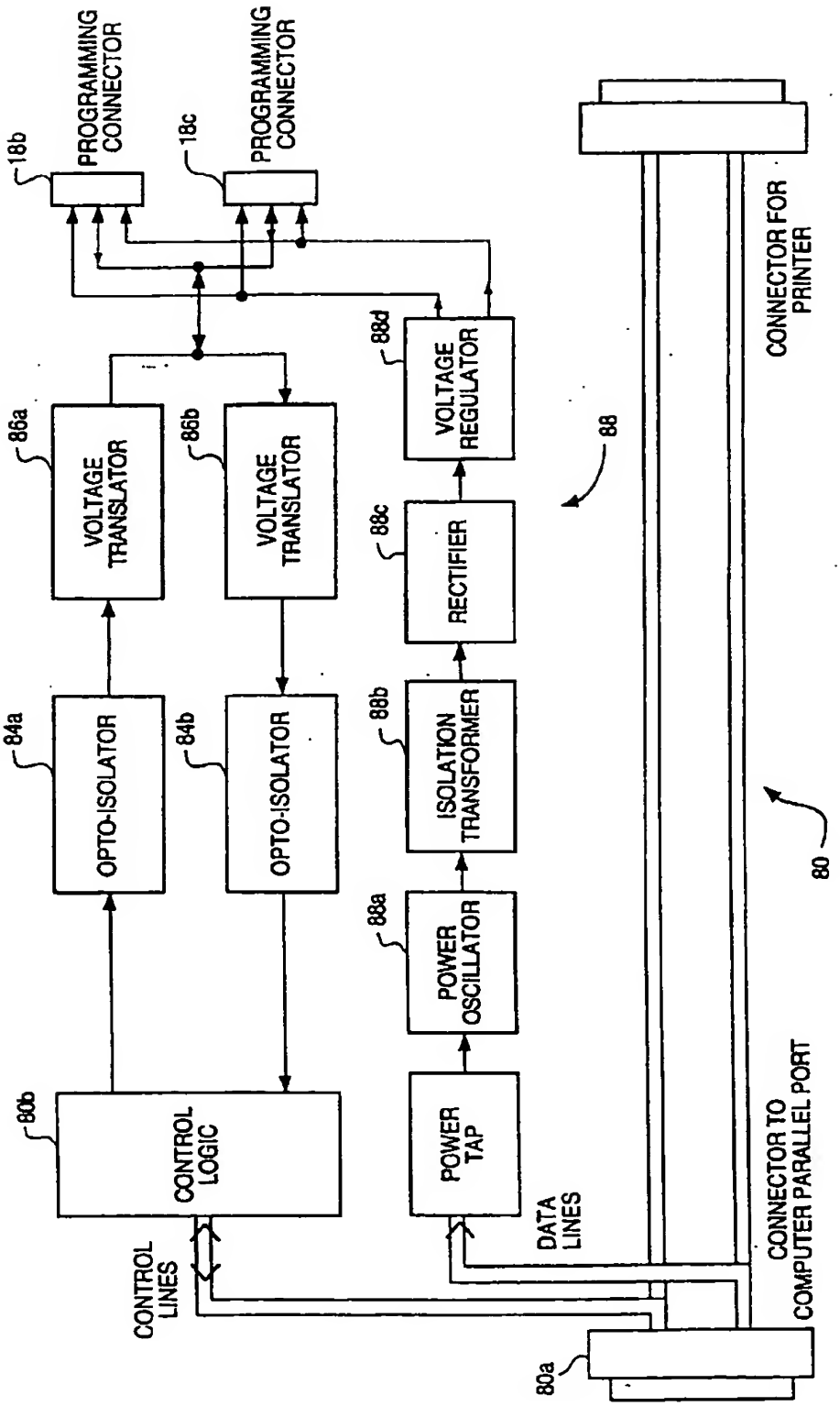


Fig. 10a



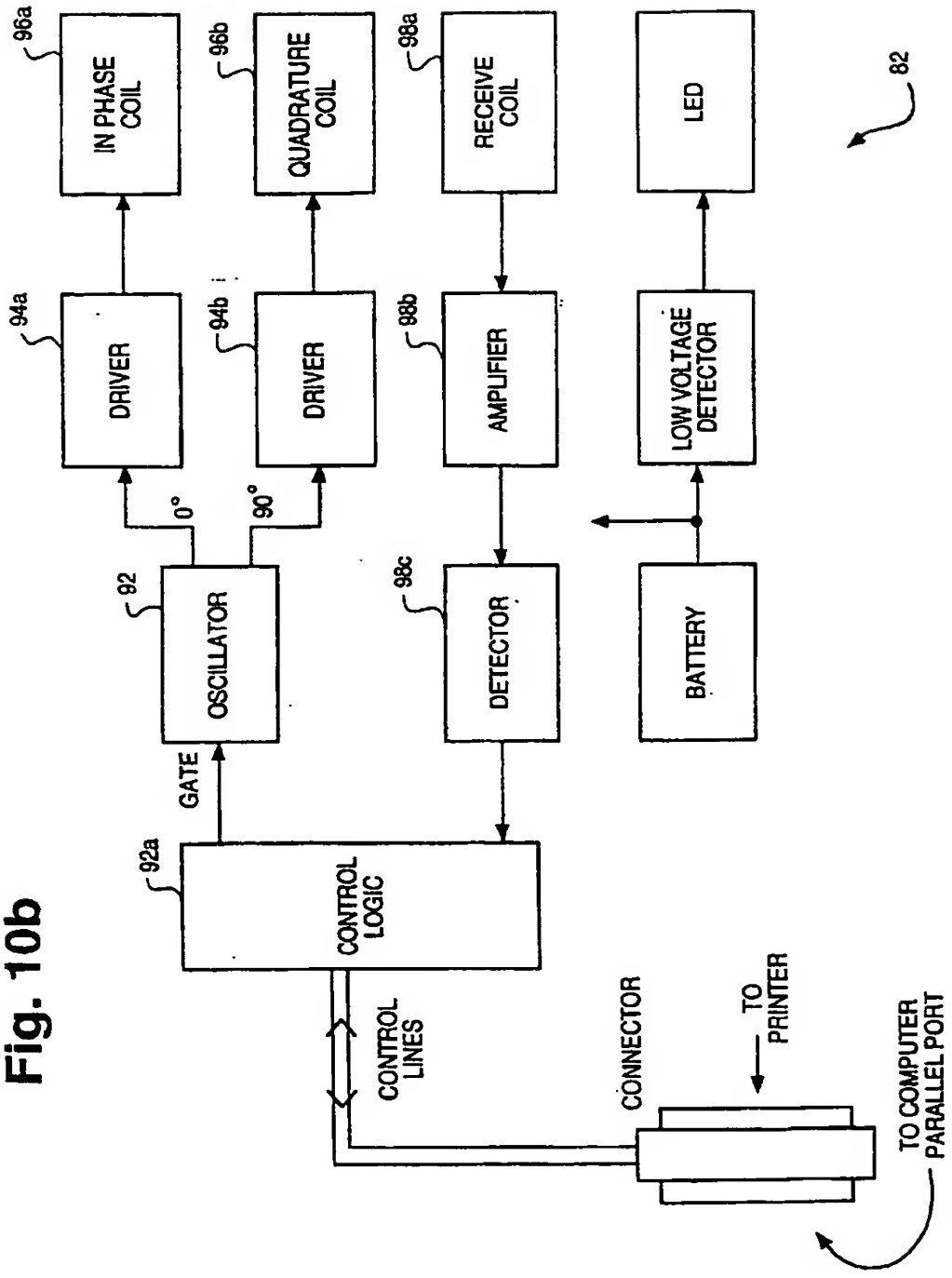


Fig. 10b